CLB Slices: 4372  
LUTs: 2350  
Flip-Flops: 4372  
DSP Slices: 0  
TCLK = 3.338 ns  
Minimum Latency: (256/8)\* 3.338ns = 106.816ns  
With a minimum latency of 106.816ns to return 32 bits of information per clock cycle, the maximum throughput will be: 32/(106.816 ns) = 299.58 Megabits per second